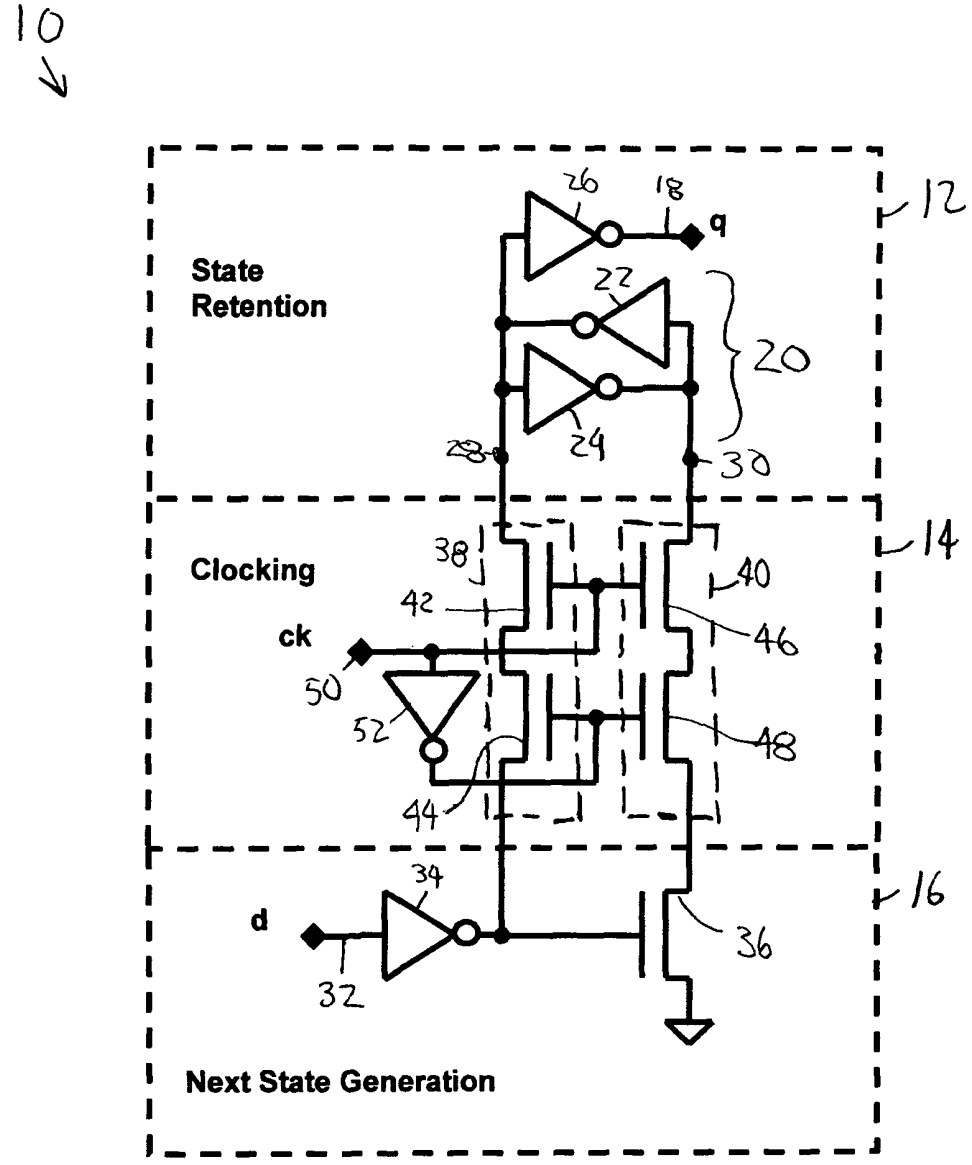
10
12
State
Retention
26
18
q
22
20
24
28
30
14
Clocking
38
40
42
ck
46
50
52
48
44
16
d
34
36
32
Next State Generation

FIG. 1

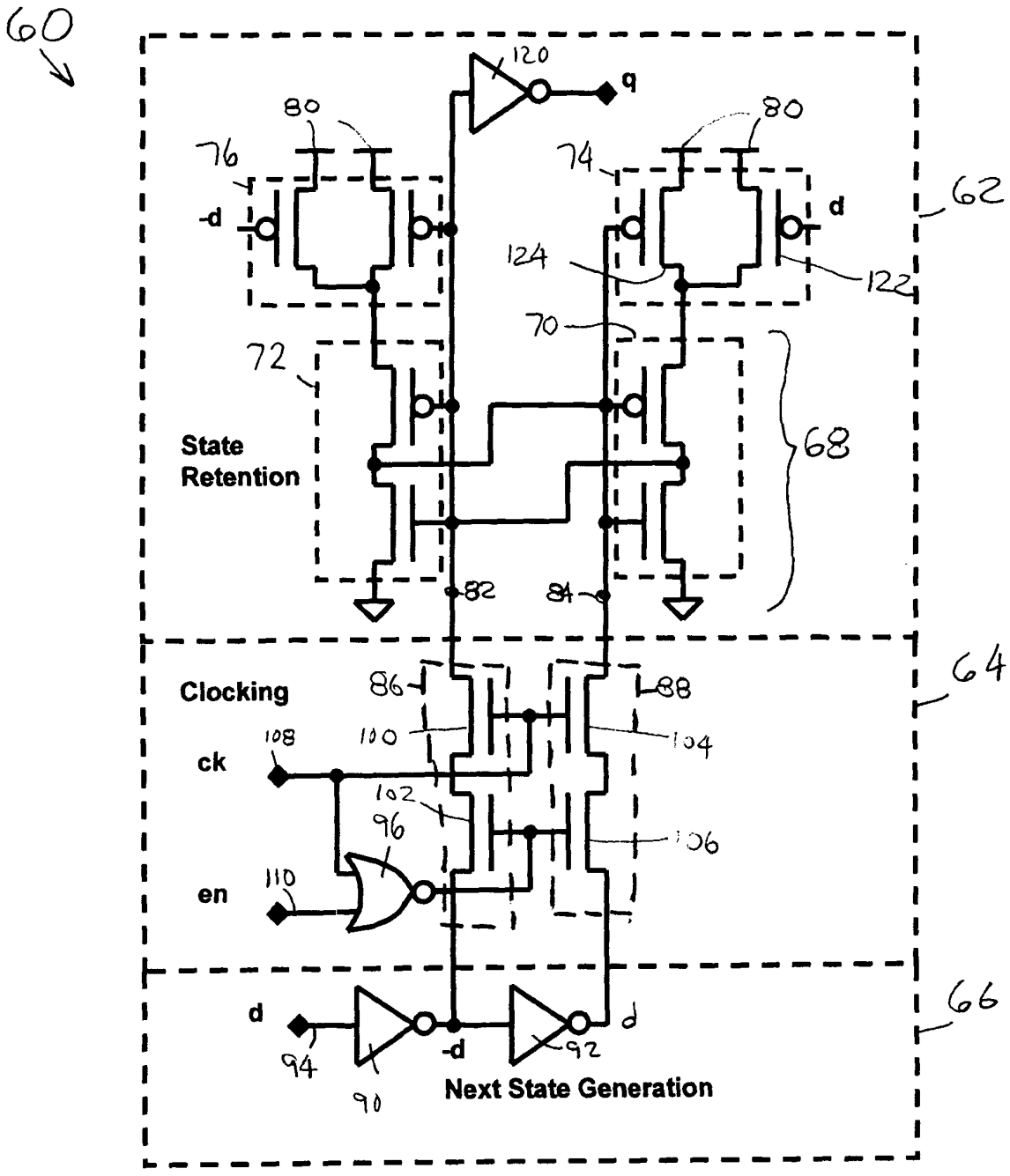
60
120
q
80
80
76
74
-d
d
62
124
122
70
72
68
State
Retention
82
84
64
Clocking
86
88
108
100
104
ck
102
96
106
110
en
66
d
94
-d
92
d
90
Next State Generation

FIG. 2

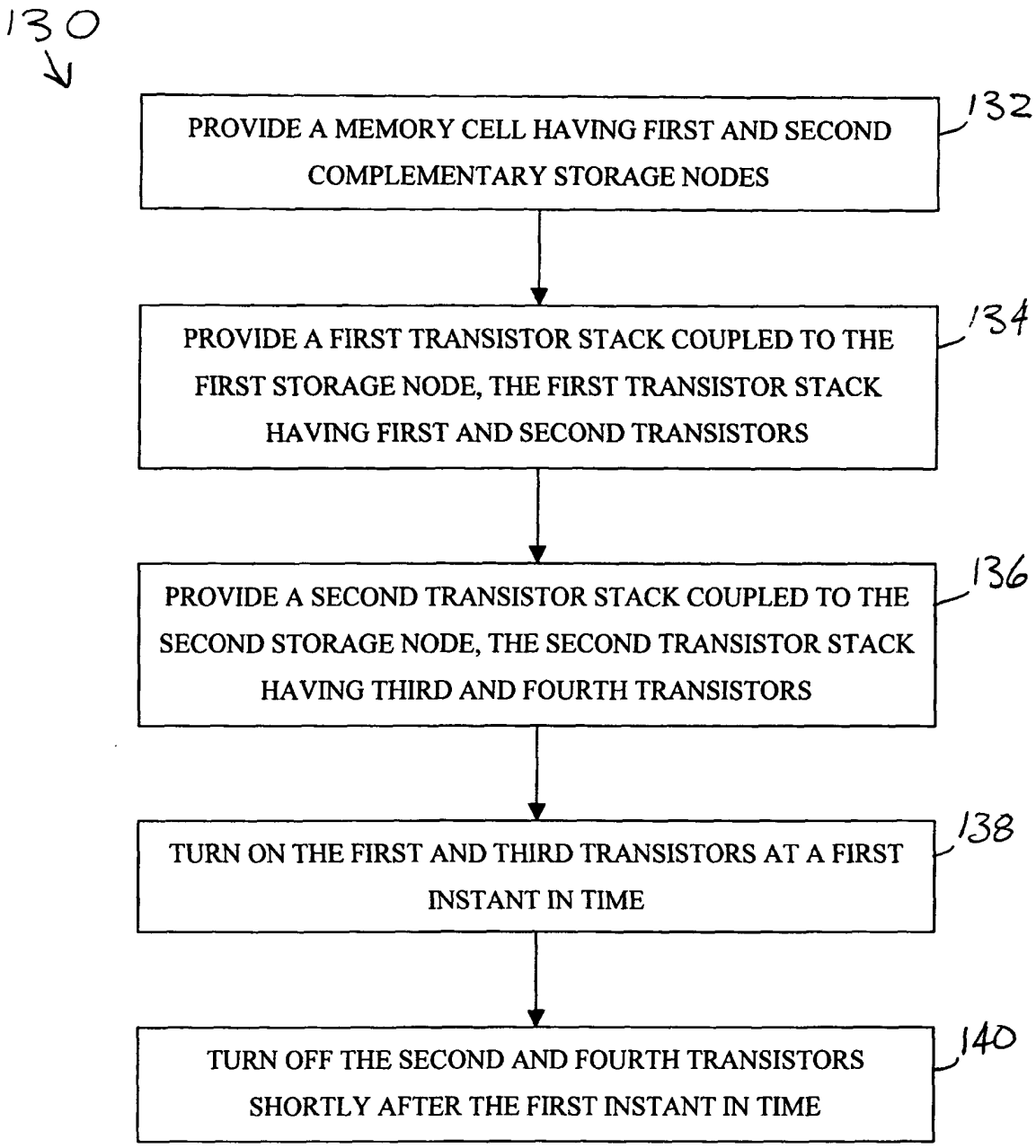
130
PROVIDE A MEMORY CELL HAVING FIRST AND SECOND COMPLEMENTARY STORAGE NODES
132
PROVIDE A FIRST TRANSISTOR STACK COUPLED TO THE FIRST STORAGE NODE, THE FIRST TRANSISTOR STACK HAVING FIRST AND SECOND TRANSISTORS
134
PROVIDE A SECOND TRANSISTOR STACK COUPLED TO THE SECOND STORAGE NODE, THE SECOND TRANSISTOR STACK HAVING THIRD AND FOURTH TRANSISTORS
136
TURN ON THE FIRST AND THIRD TRANSISTORS AT A FIRST INSTANT IN TIME
138
TURN OFF THE SECOND AND FOURTH TRANSISTORS SHORTLY AFTER THE FIRST INSTANT IN TIME
140

**Fig. 3**